ABSTRACT

[0024] The present integrated chip package provides a low cost package that is suitable for high density semiconductors that have high power dissipation. The integrated chip package includes at least one semiconductor chip having a first surface and a second surface. The first surface of the semiconductor chip is electrically coupled to an intermediate substrate via conductive bumps. The intermediate substrate is also electrically coupled to a package substrate via a plurality of bonding wires. The second surface of the semiconductor chip is thermally coupled to a heat sink to increase the power dissipation capacity of the integrated chip package.